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(54) Multichannel transceiver of digital signals over power lines

(57) A data transceiving station of digital data frames comprising a digital modem (MODEM) coupled to a transmission line, a microprocessor (μP) receiving demodulated data from said modem according to a Packet Mode or a Bit Mode transmission through an interface circuit (SERIAL_INTERFACE) that switches from a Packet Mode to a Bit Mode transmission and/or viceversa during transfer of a data frame to said microprocessor conjugating the superior speed of a Packet Mode transfer with the unlimited compatibility of a Bit Mode transfer.

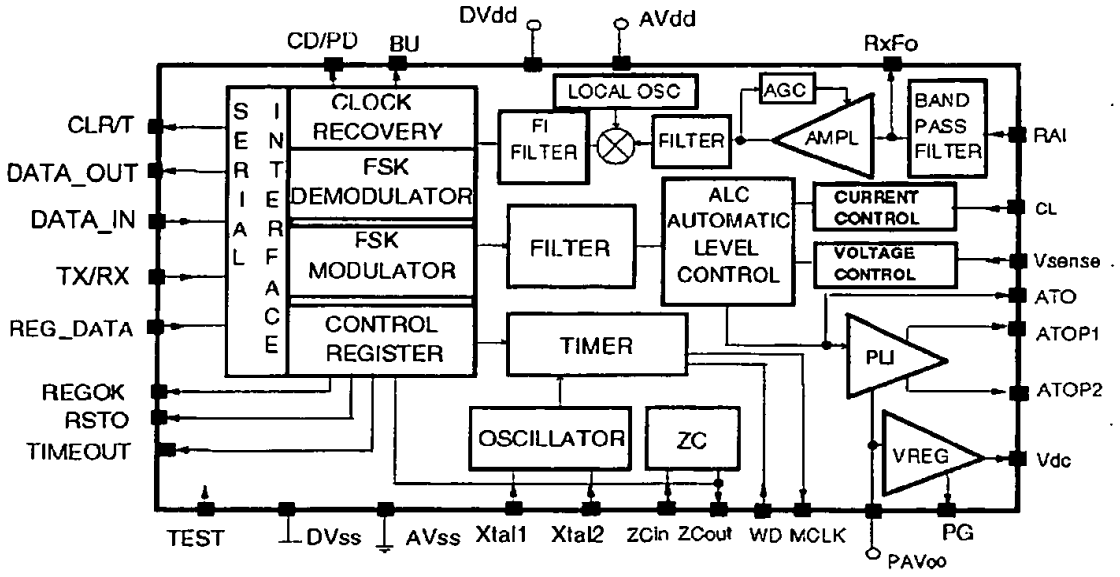

fig. 2

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Description

FIELD OF THE INVENTION

[0001] The present invention relates to data transmission systems and in particular to digital signal transceivers for home applications specially though not exclusively coupled to an electric power distribution line.

BACKGROUND OF THE INVENTION

[0002] Electric power distribution networks are widespread and capillary. Its preminent utility is for transport and distribution of electric energy, but the possibility of exploiting it also as a medium for data transmission is well known.

[0003] Electrical mains can be advantageously used to establish communication with far away locations exploiting the fact that after even remote rural users are reached by an electric power line and it is possible to avoid to cost of the dedicated line (e.g. a telephone line) for telecommunications.

[0004] Data transmission on electric mains is possible AC power is distributed with a well determined frequency. Signal modulation techniques permit to transmit information on or about a certain carrier frequency that may advantageously be in a frequency band not occupied by other signals. In such a way it is possible to transmit on a same line several signals, each occupying a different frequency band; having the receiver the possibility to select the desired signal only by turning on the relative carrier frequency.

[0005] Data transmission on power lines may be a particularly efficient technique for controlling machines installed in a remote location, without being forced to install a dedicated telecommunication line.

[0006] Because of the advantages provided by such a data transmission technique, transceivers for coupling to power lines have an increasing importance .

[0007] A telecommunication station coupled to power lines generally includes a microprocessor interfaced with a transceiver coupled to the power line.

[0008] Power line transceivers are well known and commercially available. Examples of effective transceivers are described in US Patent No. 4,714,912 and US Patent No. 5,842,032.

[0009] Generally, known transceivers are not directly interfaceable with a microprocessor, moreover the require dedicated interface device for coupling with the mains in order to meet the requisites of the communication standards on the electric network, establishing access criterions, forbidden frequency bands reserved to electricity producers and frequency bands reserved for home applications ("domotics").

[0010] It would be desirable to have a fully integrated transceiver allowing the realization of a telecommunication station with the above mentioned characteristics, capable of supporting the remote managing of electric loads connected to the power mains.

[0011] Often the conditions for using of such a telecommunication system on electric power lines are those of communicating with people at their homes, such as in applications generally referred as home applications or with the neologism "domotics".

[0012] In these application areas, the cost of apparatuses has a great importance.

[0013] Usually a digital data transceiving station, specifically destined to use a multichannel transceiver coupled through an appropriate interface to an electric power distribution network or else, generally comprises a modem interfaced with a microprocessor by way of a specific communication circuit between modem and microprocessor, commonly called "serial interface".

[0014] In known systems, the possible choices are either to establish a Bit Mode or a Packet Mode communication between modem and microprocessor, through the serial interface.

[0015] In fact, binary serial transmission between a modem and a microprocessor can be made in two different ways:

- **Bit Mode:** each time the modem has a demodulated bit, transmits it to the microprocessor;
- **Packet Mode:** the modem stores a pre-established number of bits constituting a packet of bits that eventually is transmitted to the microprocessor.

[0016] Bit Mode communication between modem and microprocessor does not introduce any data format, because bits are transmitted immediately after the modem has decoded them. It is easy to understand that the Bit Mode has the advantage of being usable irrespectively of any particular data format, but its drawback is that the rate of communication between modem and microprocessor is limited to that of the communication channel.

[0017] By contrast, in Packet Mode communication the rate of communication between modem and microprocessor can be greater than the channel's one, but it is not independent of the particular data format.

[0018] Bit Mode communication ensures compatibility of the system irrespectively of the data format used, but this solution impose the use of a microprocessor having adequate computing capacities, because it must elaborate the bitstream received by the serial interface to interpret its information content.

[0019] The technical alternative of establishing a Packet Mode communication between the modem and the microprocessor is advantageous because it ensures a faster communication and allows the use of a relatively low cost microprocessor for the same global performances of the station, but is usable only by operating with a certain predefined data format.

[0020] For example, if the protocol format the data in frames transmitted with a preamble followed by a header and by a data field alternated with synchronism sig-

nals, formatting the preamble into packets would destroy its information content. If data were formatted in M bit words and the Packet Mode transmission constitutes packets of N bits, the microprocessor would be forced to process the received data in order to extract the original M bit words, thus wasting the benefits of the greater communication speed that may be achieved with a Packet Mode transmission.

[0021] Therefore, there is a clear need and/or utility of having a digital data transceiver wherein communication between modem and microprocessor through the serial interface may switch from a Bit Mode to a Packet Mode and viceversa during the time slot in which a single data frame is transmitted, without any loss of data.

OBJECT AND SUMMARY OF THE INVENTION

[0022] It has been found and is the object of the present invention a digital data transceiving station conjugating in an optimal manner the advantages of a Packet Mode transmission with the advantages of a Bit Mode transmission, thus providing enhanced speed performances even using a relatively low cost microprocessor.

[0023] The transceiving station of the invention is characterized in that during the transmission of each single data frame between modem and microprocessor and viceversa, the serial interface switchs from a Packet Mode to a Bit Mode communication without losing data.

[0024] According to a preferred embodiment of the invention, the data transceiver of the invention is directly connectable to coupling circuit to a line of a power distribution network by means of an integrated interface circuit and the modem produce an information of detection, in a selected transmission band, of a signal energy level greater than a pre-established threshold level.

[0025] Preferably, the integrated data transceiver of the invention also comprises a circuit that detects the zero crosses of the power network voltage, producing a logic signal that is input to the modem.

[0026] According to another aspect of the invention, the station is based on the use of a monolithically integrated multichannel transceiver of digital data on a line of a power distribution network, comprising a modem having a register for data storage and means for controlling their integrity and signalling any the eventual corruption of at least one bit, a serial interface for communicating with an external microprocessor, an oscillator generating carrier frequencies that are fed to the modem, a power line interface circuit coupled to the modem, driving an external circuit of coupling with the power line and a circuit detecting the zero-crosses of the network voltage and producing a logic signal that is fed to an input of the modem.

[0027] According to the present invention, the data transmission section of the serial interface of the transceiver includes a buffer and logic circuit that processes the demodulated bitstream coming from the modem. The logic circuit is enabled by an enabling signal and functions with a clock of a frequency multiple of the demodulated bitstream frequency, the enabling signal and the multiple clock signal are both generated by control logic circuit of the serial interface, in function of a command issued by an external microprocessor.

[0028] A multiplexer receives on a first input the non-formatted bitstream output by the modem and on a second input a packet reorganized data flow produced by the processing circuit.

[0029] The same enabling signal of the processing circuit operates also the selection by the multiplexer, outputting towards the external microprocessor a bitstream (Bit Mode) as decoded by the modem or a flow of data organized in packets (Packet Mode) from the processing circuit.

BRIEF DESCRIPTION OF DRAWINGS

[0030] The different aspects and advantages of the invention will be evidenced in the following description of embodiments of the invention and by referring to the attached drawings, wherein:

Figure 1 is a general diagram of the integrated transceiver of the invention;

Figure 2 is a more detailed diagram of certain blocks of the general diagram of Fig. 1, according to an embodiment of the invention;

Figure 3 is a block diagram of the serial interface of the integrated transceiver of the invention;

Figure 4a is the circuit diagram embodiment of the transmitting section of the serial interface of the transceiver of the invention;

Figure 4b is a diagram of important signals of the transmitting section of the serial interface of Fig. 4a;

Figure 5a depicts a transceiving station coupled to a power distribution line;

Figure 5b depicts a possible circuit for coupling the transceiver of the invention to a power network line.

DESCRIPTION OF EMBODIMENTS OF THE INVENTION

[0031] The integrated transceiver of the invention is depicted schematically in Fig. 1. IT is constituted by a digital modem MODEM, for example a Frequency Shift Keying (FSK) modem, a serial interface circuit SERIAL_INTERFACE of communication of the modem with the external world, an oscillator OSCILLATOR providing carrier frequencies to the modem, a power interface PLI for driving an external coupling circuit to a line of the electric power distribution network and a zero-

cross detector ZC of the network voltage.

[0032] Optionally, a monolithically integrated voltage regulator VREG is also present for powering other ICs that may be present in the transceiving station.

[0033] During a receiving phase, the signal derived from the power network line is received on the pin RAI, demodulated and made available on the pin DATA_OUT. Optionally, the transceiver may produce on the pin CLR/T a clock signal of bit synchronism.

[0034] The integrated transceiver provides on the pin BU information about the detection of an energy level greater than a fixed threshold, e.g. 80dBμV, in a selected frequency band. Such information allows the use of the communication channel on an electric power line in the frequency band reserved to home applications. According to the CENELEC EN 50065-1 rules, defining the European criteria for the access to such a telecommunication medium, it is forbidden to transmit in the frequency band reserved to home applications if on the channel there is a signal stronger than 80dBμV. By having the modem implementing this energy detection function in a selected band, realization of dedicated external circuitry for filtering and amplitude monitoring is avoided.

[0035] Another peculiarity of the integrated circuit of the invention is the fact that it integrates a circuit, ZC, that detects the zero-crosses of the network voltage by comparing a replica signal of the network voltage fed to the pin ZCIN. The zero-cross information is produced on the pin ZCOUT and besides making it available to the external world (microprocessor) it is input to the modem for synchronizing the transmission with the zero-crosses of the network voltage.

[0036] In this way, appliances connected to the electric power network, besides receiving command data sent by the transceiver, receive also the information of the instant in which the network voltage is zero. Such information is useful to drive certain electric loads knowing the instant in which the network voltage is zero may be usefully exploited for determining the turn-on and turn-off instants of loads, thus avoiding voltage peaks on power switches. When there is not need to synchronize the transmission with the zero-crosses of the network voltage, the transceiver may be programmed to ignore the relative signal on the ZCOUT mode.

[0037] A preferred embodiment of the integrated transceiver of the invention is depicted in Fig. 2, wherein different blocks constituting the modem, which in the example of embodiment is of FSK kind, are highlighted.

[0038] The signal present on the pin RAI is demodulated by means of a receiver, for example a supereterodine receiver, in the embodiment depicted in the figure and the demodulated signal is fed to a CLOCK_RECOVERY block.

[0039] The signal present on the pin RAI, is filtered and made available, after the Band Pass Filter, on the pin RxFo providing a measure of the power of the signal in the selected band.The pin CD/PD of the transceiver of the invention has two functions. Through this pin the presence of a carrier in the selected channel (Carrier Detection), can be signalled independently of the amplitude of the carrier, for communicating the possibility that a message could be arriving. The detection threshold is determined by the modem sensibility at the input pin RAI. The other function is to communicate that a bitstream is being received with the selected bitrate (Preamble Detection).

[0040] Upon recovering the clock signal, the block FSK_DEMODULATOR provides the demodulated signal to the SERIAL_INTERFACE, block which outputs it on the pin DATA_OUT.

[0041] The SERIAL INTERFACE block conveys data from the FSK_DEMODULATOR to the outside world and from the outside world to the FSK_MODULATOR, under control of a signal TX/RX specifying which one of the two operations must be carried out.

[0042] Moreover, the transceiver is provided with a control register CONTROL_REGISTER where the parameters necessary to the transceiving, which define the modem configuration are stored.

[0043] Because of the high electromagnetic noise that is normally present on the power line, the content of the CONTROL_REGISTER is continuously monitored to ensure a reliable security margin on the integrity of the data stored in it. In case of corruption of the stored data, an alarm signal is produced on the pin, REG_OK.

[0044] Moreover, the CONTROL_REGISTER is provided with a pin, TIMEOUT, support the use of protocols that contemplate the interruption of the transmission at pre-established time intervals, as measured by the block TIMER.

[0045] The CONTROL_REGISTER can be externally programmed by way of the control signal, REG_DATA. Such a signal communicates to the SERIAL_INTERFACE whether the signal DATA_IN, coming from outside is a datum to store in the CONTROL_REGISTER or is a datum to be fed to the FSK_MODULATOR. By programming the CONTROL_REGISTER it is possible to make the information on Preamble Detection available on the pin CD/PD.

[0046] The signal produced by the FSK_MODULATOR is filtered by a programmable band pass filter, FILTER, which reduces all undesired harmonic components in order to reduce the electromagnetic noise. The filtered signal is input to the power interface PLI by way of an amplitude control stage ALC.

[0047] Regulation of the voltage level and of the current level of the transmitted signal is performed by the relative blocks of current mode control CURRENT_CONTROL and of voltage mode control VOLTAGE_CONTROL, in function of the signals representative of the current, CL, and of the voltage, VSENSE.

[0048] The transmission carrier frequencies are derived from the oscillation of an external quartz, coupled

to the pins XTAL1 and XTAL2, kept in resonance by an excitation circuit integrated in the device. Preferably, the excitation circuit includes a MOS stage operating below its threshold level, such to limit absorption. From the oscillator is derived a clock signal that is made available on the pin MCLK in order to drive an external microprocessor for optionally avoiding use of other resonators.

[0049] Preferably, the transceiver has a pin WD dedicated to the supervision of the transmission. In order to preserve the communication channel, the transceiver monitors the signal present on the pin WD: if during a pre-established time interval, as measured by the block TIMER, no transition has been observed, the control register interprets this fact as a failure and communicates to the external world an alarm by way of the signal RSTO.

[0050] The signal RSTO can be conveniently used even to signal the presence of a voltage level, as produced by the regulator VREG, insufficient to make the transceiver station operate correctly. To this effect, the voltage regulator VREG is provided with a pin PG, on which the information of the presence of an output voltage of the regulator VREG greater than a minimum pre-established value, for example 4,5V, is provided.

[0051] In Fig. 2 are indicated the supply pins for the digital and analogic sections: DVdd, DVss, AVdd, AVss and the supply pin of the power interface PAVcc. The pin TEST, is used for functionality, testing of the integrated device.

[0052] A diagram of the SERIAL_INTERFACE block is depicted in Fig. 3. It comprises a receiving section, RX_SECTION, a transmitting section, TX_SECTION, and a SERIAL_INTERFACE_CONTROL_UNIT. The line SIGNAL_GROUND provides the reference voltage for data reading.

[0053] The receiving section, RX_SECTION, receives a data signal DATA_IN and produces an output signal, DATA_SEND, that is fed either to the FSK_MODULATOR block or to the CONTROL_REGISTER, depending on the control signal REG_DATA.

[0054] The TX_SECTION comprises a logic processing circuit BUFFER_CONTROL_UNIT employing a work memory, BUFFER, and an output MULTIPLEXER.

[0055] The BUFFER_CONTROL_UNIT receives the bitstream, RECOVERED_DATA, output by the demodulator at a certain clock frequency, RECOVERED_CLOCK, and uses a clock signal BURST_CLOCK of frequency generally multiple of the frequency of the clock of the received bitstream, in order to perform data organization in packets, according to a certain format.

[0056] When enabled by the enabling signal, BURST_ENABLE, the logic processing circuit, BUFFER_CONTROL_UNIT, reads the data stored in the work memory, BUFFER, at the scanning frequency of the BURST_CLOCK and produces on an input of the MULTIPLEXER a data stream BC, organized according to a Packet Mode format.

[0057] The input bitstream, RECOVERED_DATA, besides to the logic processing circuit, is also fed to a second input of the MULTIPLEXER.

[0058] The SERIAL_INTERFACE_CONTROL_UNIT besides activating alternately the receiving section RX_SECTION, and the transmitting section, TX_SECTION, depending on an external command TX/RX, produces the signal BURST_ENABLE and the clock signal BURST_CLOCK with a frequency multiple of the clock frequency of the bitstream, that is used by the BUFFER_CONTROL_UNIT and by the MULTIPLEXER to operate the mode selection.

[0059] Optionally, even a clock signal (CLR/T) relative to the selection of a data flow in Bit Mode or in Packet Mode can be output. In this case, the logic processing circuit, BUFFER_CONTROL_UNIT, feeds to other inputs of the MULTIPLEXER a third clock signal A, constituted by sequences of a pre-established number of pulses of the BURST_CLOCK, periodically generated at pre-established intervals, and the clock of the input bitstream, RECOVERED_CLOCK.

[0060] The BURST_ENABLE signal enables or disables the logic processing circuit BUFFER_CONTROL_UNIT and select, by means of the MULTIPLEXER, the output data stream DATA_OUT, corresponding to the input bitstream (Bit Mode) RECOVERED_DATA and optionally also the relative clock RECOVERED_CLOCK on the CLR/T output, or to the BC stream of data organized in packets (Packet Mode) by the BUFFER_CONTROL_UNIT and optionally also the relative clock signal A on the CLR/T output.

[0061] An effective embodiment of the transmitting section, TX_SECTION, of the serial interface is depicted in Fig. 4a.

[0062] The circuit is composed of a pair of shift registers: SHIFT_REGISTER_I and SHIFT_REGISTER_2, having capacity equal to a bit length N of a packet. The two registers are paralleled, fed with the RECOVERED_DATA bitstream and their outputs are coupled to respective inputs of the multiplexer MUX3. The two registers store and unload the bits constituting a packet.

[0063] Data storage is performed at a frequency equal to the bitstream frequency, RECOVERED_CLOCK, while the data unloading is performed at the multiplied frequency of the BURST_CLOCK. A switching signal T, produced by the logic block TOGGLE, prevents the two registers, SHIFT_REGISTER_1 and SHIFT_REGISTER_2, from performing the same operation at the same time, and ensures that the multiplexer MUX3 coupled to the outputs of the registers coordinately selects the output of the register that is unloading the stored datum.

[0064] The signal T switches every N pulses of the RECOVERED_CLOCK, making the input multiplexers MUX1 and MUX2 feed the respective shift register, one in synchronism with the RECOVERED_CLOCK and the

other with a third clock signal A.

[0065] The modulus N first counter, COUNTER_1, enabled by the BURST_ENABLE, outputs a first end-computation signal C1 every N pulses of the RECOVERED_CLOCK. The first end-computation signal C1 makes the signal T switch and enables the modulus N counter, COUNTER_2, that produces a second end-computation signal C2, activated at the instant the counter is enabled for as long as N pulses of the BURST_CLOCK have been counted. Upon counting N pulses, COUNTER_2 disables the signal C2.

[0066] The third clock signal A is produced by performing a logic AND of the second end-computation signal C2 and of the BURST_CLOCK. Therefore the clock signal A corresponds to the period of sequences of N pulses of the BURST_CLOCK repeating at each activation of the first end-computation signal C1.

[0067] Therefore, the multiplexers MUX1 and MUX2 are fed with a signal consisting of N pulses of the BURST_CLOCK at the instant in which one of the two registers is full. By means of the switching signal T, the N pulses are input to the register that has just reached the full state, thus unloading the packet constituted by the N bits stored in it.

[0068] If it is contemplated to output also the clock signal CLR/T with which bits are output as DATA_OUT, according to the selection operated between the Bit Mode and Packet Mode, it can be produced by means of a multiplexer MUX4 for outputting either the RECOVERED_CLOCK or the third clock signal A, depending on whether the signal BURST_ENABLE establishes a Bit Mode or a Packet Mode transmission.

[0069] An output multiplexer MUX5 outputs the bit-stream DATA_OUT in Packet Mode or in Bit Mode, according to the selection operated by the signal BURST_ENABLE.

[0070] The described architecture is just one among many realizable ones according to the diagram of Fig. 3. Other circuital solutions are possible, for example by using a RAM memory or a circular register instead of the pair of shift registers and by adapting the BUFFER CONTROL_UNIT such to produce the appropriate signals to manage the particular type of storage means used.

[0071] The above described SERIAL_INTERFACE allows to switch between Bit Mode and Packet Mode data transmission to the microprocessor by just varying the BURST_ENABLE signal during transmission of a data frame.

[0072] This ability allows the transmission of the message to be sent exploiting both the versatility of a Bit Mode transmission and the superior speed of a Packet Mode transmission, for example by transmitting a portion of the data frame in Bit Mode and the remaining portion in Packet Mode, and even alternating the two modes of transmission in whichever order causing any bit loss while switching from a transmission mode to the other.

[0073] A timing diagram of the most important signals of the serial interface is depicted in Fig. 4b.

[0074] Generally, a data frame FRAME of the stream DATA_OUT can be split into a PREAMBLE, a HEADER and in a payload portion containing the data bits DATA, interleaved by synchronism signals CRC.

[0075] The signal TX/RX switches, so enabling the TX_SECTION of the SERIAL_INTERFACE. Given that it is not possible to transmit the bits belonging to the PREAMBLE and/or to the HEADER in Packet Mode, because the information carried is in their bit-rate, the BURST_ENABLE signal switches in order to transmit the PREAMBLE and the HEADER in Bit Mode and the data bits DATA in Packet Mode.

[0076] Such a switching from a transmission mode to the other is not the only possible switching scheme. It is possible to command any number of switchings from Packet Mode to Bit Mode and viceversa during the transmission of a single data frame FRAME.

[0077] During transmission in Packet Mode, the clock signal CLR/T is idle in certain time intervals, allowing the reading of the signal DATA_OUT only when the above mentioned sequences of N pulses of the BURST_CLOCK are present. This is highlighted in the enlarged detail of Fig. 4b, wherein the DATA_OUT signal is read only when the CLR/T clock is not idle, and as depicted by way of an example in correspondence of its rising edge.

[0078] A sample scheme of a circuit of a transceiving station according to the present invention is depicted in Fig. 5a.

[0079] Substantially, the transceiving station is realized with the transceiver of Fig. 2.

[0080] Fundamentally, the receiving station comprises a digital modem coupled to a data transmission line that in the example shown in figure is a line of a power distribution network. A microprocessor μP receives the data demodulated by the modem in Packet Mode or in Bit Mode through the interface circuit SERIAL_INTERFACE that couples the modem to the microprocessor μP. The SERIAL_INTERFACE changes the transmission mode to the microprocessor of the demodulated data from a Packet Mode to a Bit Mode during the transmission of each single data frame, without any bit loss during the switching from a mode to the other.

[0081] A suitable circuit to couple the transceiver of the invention to the electric power line is depicted in Fig. 5b.

[0082] The station may me made able to control electric loads connected to the power line by using the frequency bands that are reserved for this function. The station monitors the presence in the selected band of an energy level greater than a certain pre-established maximum threshold and accesses to the transmission channel only if such a pre-established threshold may be equal to 80dBμV, meeting the requirements of CENELEC EN 50065-1 rules that define the European

standard in accessing electric power lines for communications relative to home applications.

[0083] In order to improve the control of electric loads, avoiding undesired overvoltages on switches, the integrated transceiver of the invention includes a circuit, ZC, for detecting the zero-crosses of the network voltage.

Claims

1. A data transceiving station of digital data frames comprising a digital modem (MODEM) coupled to a transmission line, a microprocessor (μP) receiving demodulated data from said modem according to a Packet Mode or a Bit Mode transmission, an interface circuit (SERIAL_INTERFACE) between said microprocessor (μP) and said digital modem (MODEM) characterized in that

   said interface circuit (SERIAL_INTERFACE) switches from a Packet Mode to a Bit Mode transmission and/or viceversa during transfer of a data frame to said microprocessor.

2. The data transceiving station of claim 1, wherein said transmission line is a line of an electric power distribution network and said modem (MODEM) generates an information on the detection of an energy level greater than a pre-established threshold in a frequency band selected for transmission over said line.

3. The data transceiving station of claim 2, characterized in that it comprises a circuit (ZC) detecting the zero-crosses of the network voltage and producing a logic signal (ZCOUT) that is also input to said modem (MODEM).

4. A monolithically integrated multichannel transceiver of digital frames over a line of an electric distribution power network, comprising a modem (MODEM) having a register for data storage (CONTROL_REGISTER) and means for controlling their integrity and signalling any eventual corruption of at least one bit, a serial interface (SERIAL_INTERFACE), including a receiving section (RX_SECTION) and a transmitting section (TX_SECTION), coupling said modem to the external world, an oscillator (OSCILLATOR) generating carrier frequencies fed to said modem, a power interface circuit (PLI), coupled to said modem and driving an external coupling circuit to said line, characterized in that it comprises

   a circuit (ZC) detecting the zero-crosses of the network voltage and producing an output logic signal (ZCOUT) coupled to an input of said modem (MODEM) and to a pin of the transceiver;

   said modem detecting the energy level in a certain frequency band selected for transmission over said line, producing a logic signal on a dedicated pin (BU) when said energy level surpasses a pre-established threshold;

   said transmitting section (TX_SECTION) of the serial interface (SERIAL_INTERFACE) comprises a logic processing circuit (BUFFER_CONTROL_UNIT) and a work memory (BUFFER) for organizing a demodulated bitstream (RECOVERED_DATA)coming from the modem in a stream (BC) of data structured in packets, a multiplexer (MULTIPLEXER) receiving on a first input said demodulated bitstream (RECOVERED_DATA) and said stream of structured data (BC) and operating a selection between said two streams outputting (DATA_OUT) either a not structured Bit Mode bitstream or a Packet Mode data stream organized in packets, in function of a selection signal (BURST_ENABLE) and a control unit (SERIAL_INTERFACE_CONTROL UNIT) producing said selection signal (BURST_ENABLE) and a clock signal (RECOVERED_CLOCK) of said input bitstream (RECOVERED_DATA).

5. The transceiver of claim 4 wherein

   said logic circuit processing (BUFFER_CONTROL_UNIT) produces a third clock signal (A) constituted by sequences of N pulses of a second clock signal (BURST_CLOCK) having frequency multiple of the frequency of said clock signal (RECOVERED_CLOCK) of the input bitstream at pre-established intervals;

   said multiplexer (MULTIPLEXER) receives said clock signal (RECOVERED_CLOCK) of the input bitstream (RECOVERED_DATA) and said third clock signal (A), outputting a fourth clock signal (CLR/T) equal to said third clock signal (A) or to said first clock signal (RECOVERED_CLOCK) depending on whether said selection signal (BURST_ENABLE) selects said not structured bitstream (RECOVERED_DATA) or said data flow structured in packets (BC).

6. The transceiver of claim 4 wherein

   said work memory (BUFFER) comprises

   a first register (SHIFT_REGISTER_1) and second register (SHIFT_REGISTER_2) fed with said demodulated datastream

(RECOVERED_DATA), and clocked with respective clock signals (Z1, Z2), and outputting a first data signal (S1) and a second data signal (S2), respectively;

said logic processing circuit (BUFFER_CONTROL_UNIT) comprises

a first modulus N counter (COUNTER_1) fed with said first clock signal (RECOVERED_CLOCK) producing a first end-computation signal (CI) when N pulses have been counted,

a second modulus N counter (COUNTER_2) fed with said second clock signal (BURST_CLOCK) and enabled by said first end-computation signal (CI), producing a second end-computation signal (C2) that is enabled by said first end-computation signal (C1) and disabled when said second counter (COUNTER_2) counts N pulses of said second clock signal (BURST_CLOCK),

a second multiplexer (MUX_1) and third multiplexer (MUX_2) fed with said demodulated bitstream (RECOVERED_DATA) and with said third clock signal (A) producing respectively said clock signals (ZI, Z2) corresponding alternately to said third clock signal (A) and to said first clock signal (RECOVERED_CLOCK), depending on a switching signal (T),that toggles every N pulses of said first clock signal;

a logic AND gate, combining said second clock signal (BURST_CLOCK) and said second end-computation signal (C2), producing said third clock signal (A) as periodic sequences of N pulses of said second clock signal (BURST_CLOCK) output at each enablement of said first end-computation signal (C1),

a fourth multiplexer (MUX_3) fed with said first data signal (S1) and with said second data signal (S2) and outputting a third data signal (BC) corresponding

to said first data signal (S1) or to said second data signal (S2) depending on said switching signal (T).

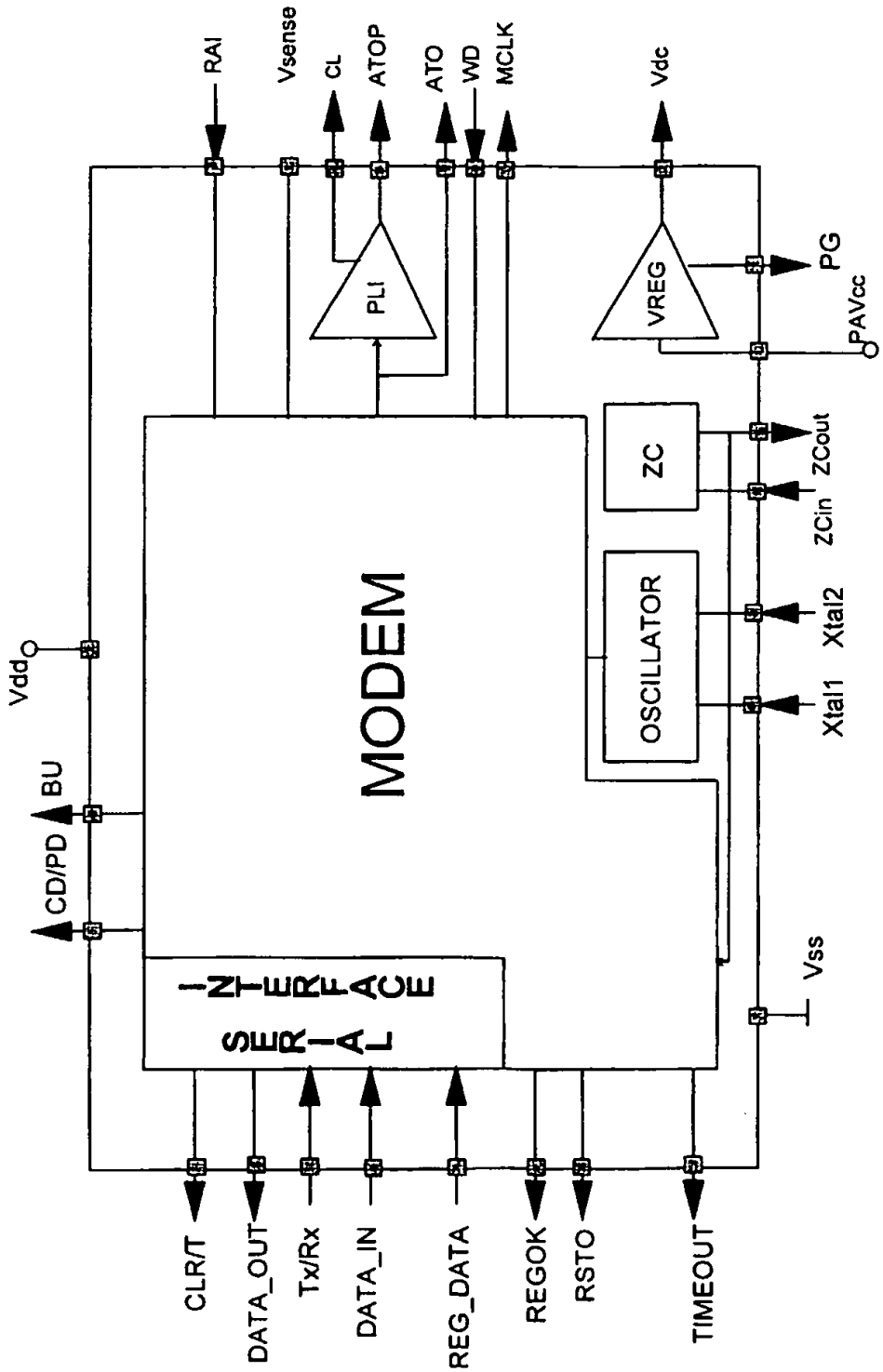
RAI
Vsense
CL
ATOP
ATO
WD
MCLK
Vdc
PLI
VREG
PG
PAVcc
ZC
ZCout
ZCin
MODEM
OSCILLATOR
Xtal2
Xtal1
Vdd
BU
CD/PD
Vss
CLR/T
DATA_OUT
Tx/Rx
DATA_IN
REG_DATA
REGOK
RSTO
TIMEOUT

fig. 1

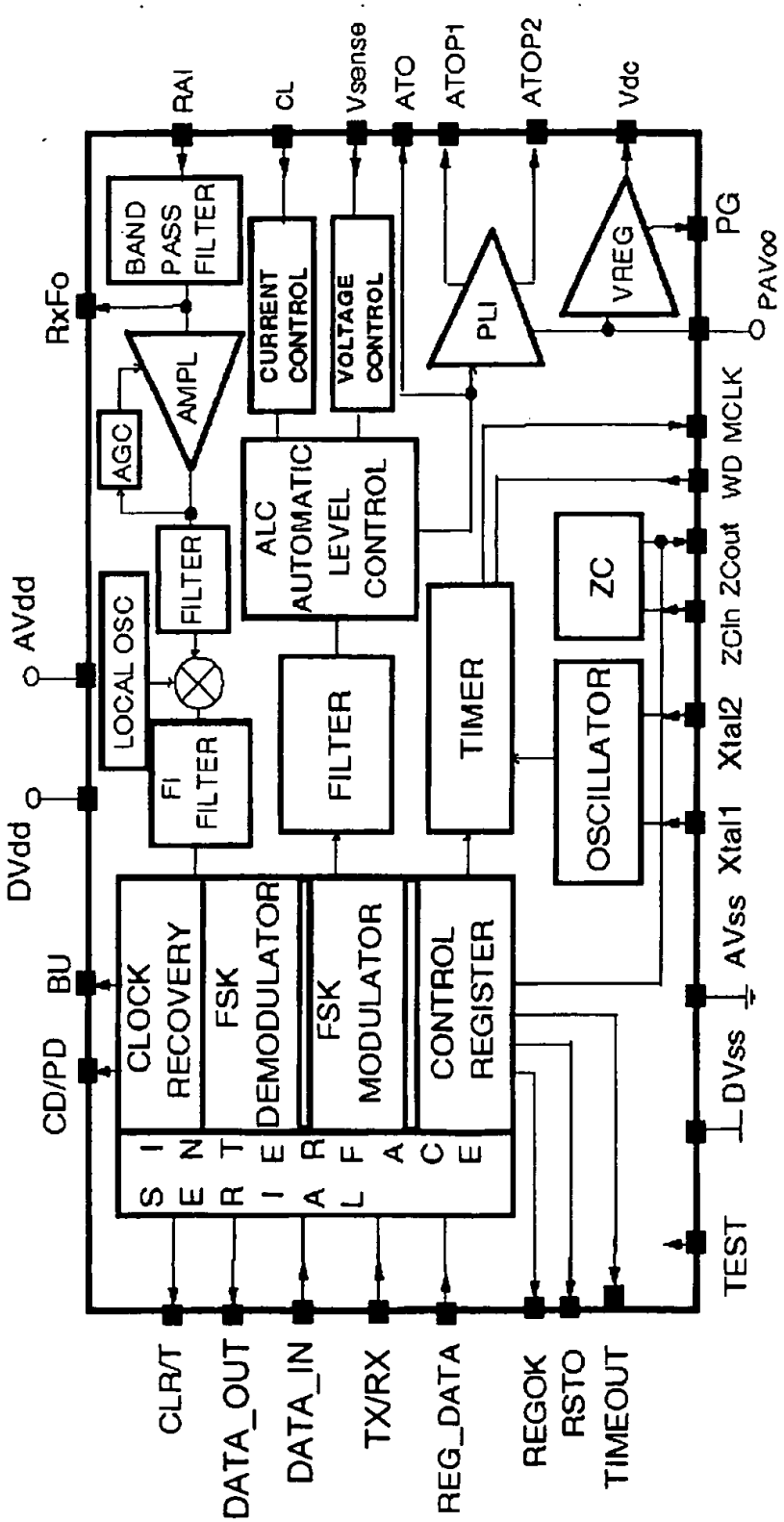
RAI
CL
Vsense
ATO
ATOP1
ATOP2
Vdc
PG
PAVoo
RxFo
BAND PASS FILTER
CURRENT CONTROL
VOLTAGE CONTROL
PLI
VREG
AMPL
AGC
ALC AUTOMATIC LEVEL CONTROL
WD MCLK
AVdd
LOCAL OSC
FILTER
ZC
ZCin ZCout
FI FILTER
FILTER
TIMER
OSCILLATOR
Xtal2
DVdd
Xtal1
BU
AVss
CD/PD
DVss
CLOCK RECOVERY
FSK DEMODULATOR
FSK MODULATOR
CONTROL REGISTER
SI EN RT IE RF AL AC E
TEST
CLR/T
DATA_OUT
DATA_IN
TX/RX
REG_DATA
REGOK
RSTO
TIMEOUT

fig. 2

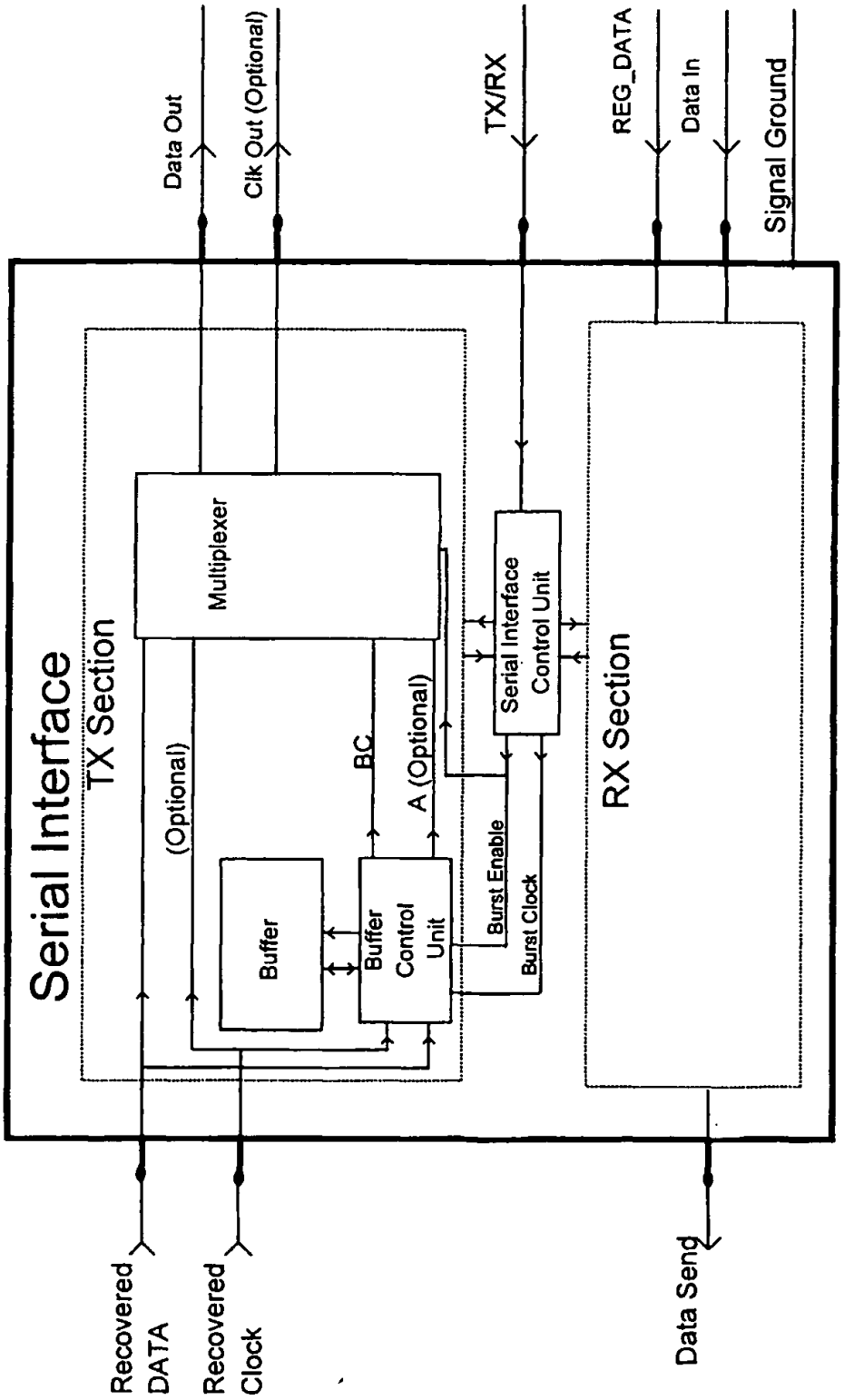
Serial Interface
TX Section
RX Section
Multiplexer
Buffer
Buffer Control Unit
Serial Interface Control Unit
(Optional)
BC
A (Optional)
Burst Enable
Burst Clock
Data Out
Clk Out (Optional)
TX/RX
REG_DATA
Data In
Signal Ground
Recovered DATA
Recovered Clock
Data Send

fig. 3

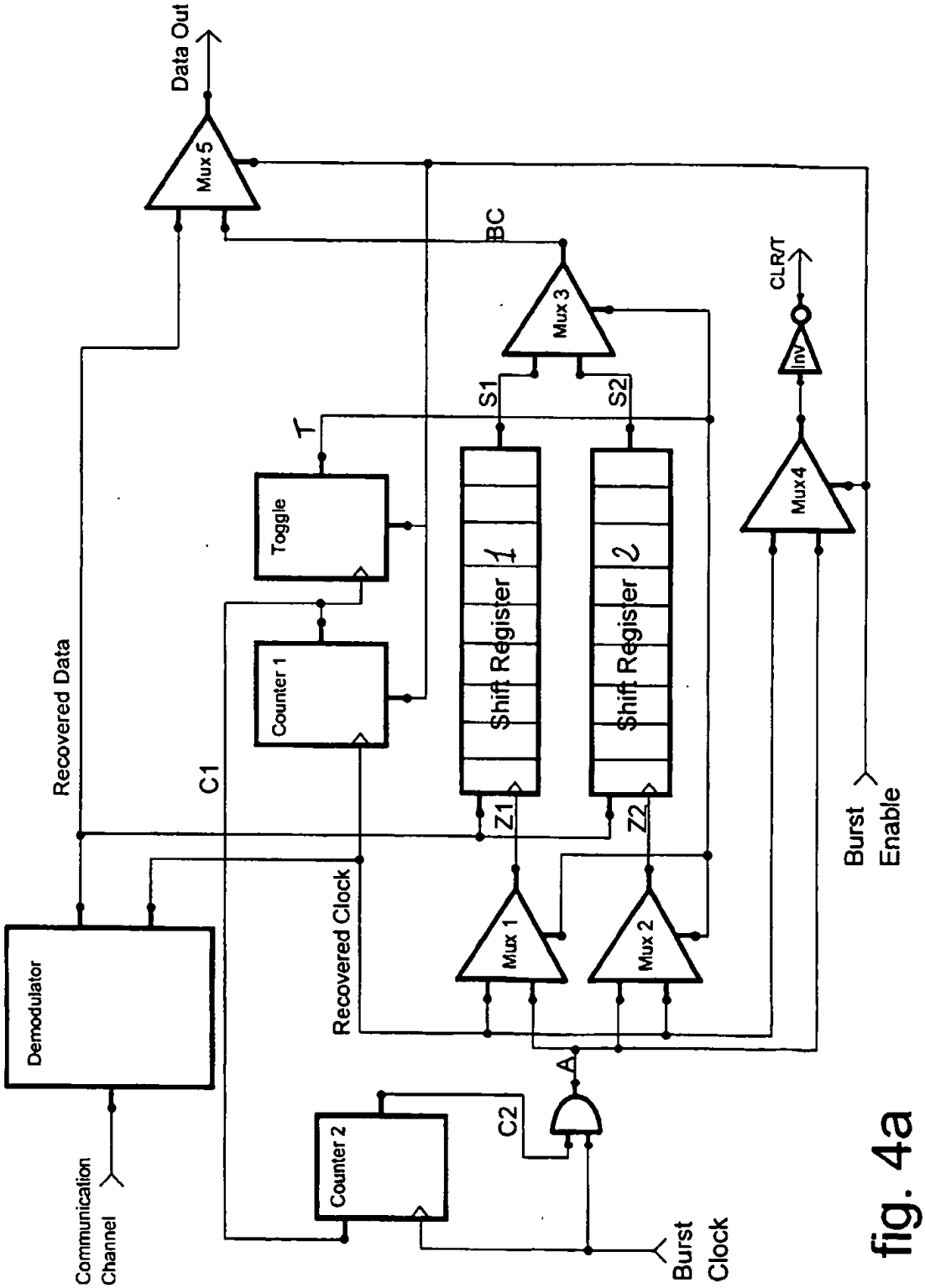
Data Out
Mux 5
BC
Mux 3
CLR/T
Inv
S1
S2
T
Toggle
Shift Register 1
Shift Register 2
Mux 4
Counter 1
C1
Recovered Data
Z1
Z2
Burst Enable
Demodulator
Recovered Clock
Mux 1
Mux 2
A
C2
Counter 2
Communication Channel
Burst Clock

fig. 4a

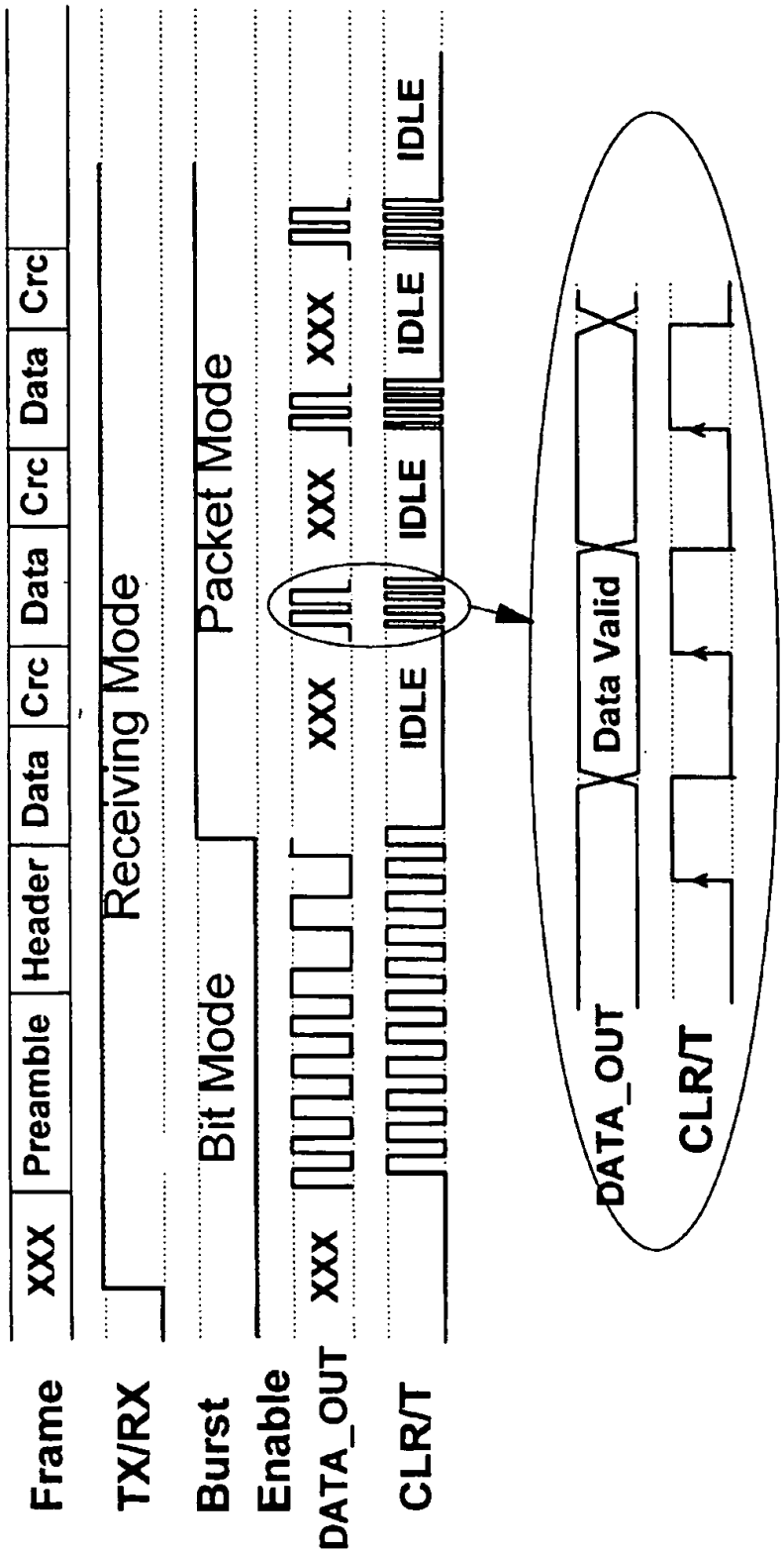
Frame
XXX
Preamble
Header
Data
Crc
Data
Crc
Data
Crc
TX/RX
Receiving Mode
Burst Enable
Bit Mode
Packet Mode
DATA_OUT
XXX
XXX
XXX
CLR/T
IDLE
IDLE
IDLE
IDLE
DATA_OUT
Data Valid
CLR/T

fig. 4b

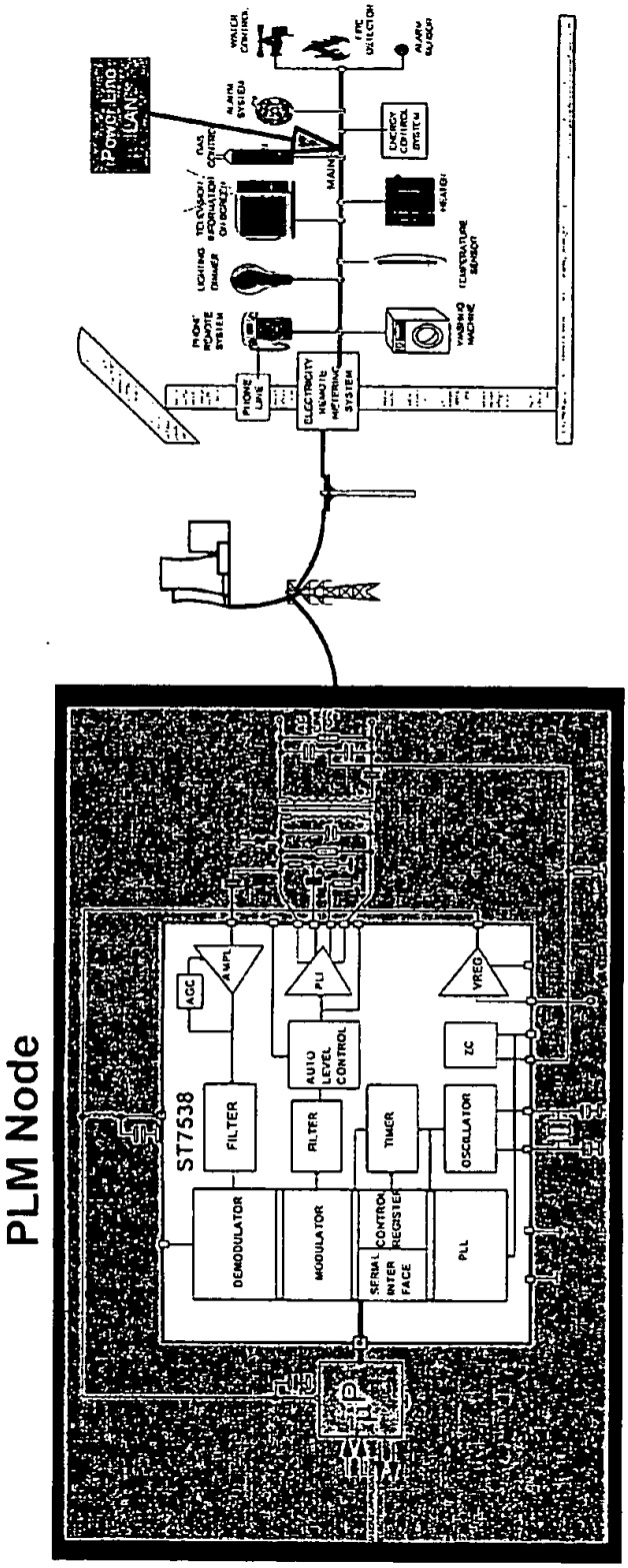
PLM Node
ST7538
AGC
AMPL
PLI
VREG
AUTO LEVEL CONTROL
ZC
FILTER
FILTER
TIMER
OSCILLATOR
DEMODULATOR
MODULATOR
SERIAL INTERFACE
CONTROL REGISTER
PLL
MAIN
PHONE LINE
ELECTRICITY REMOTE METERING SYSTEM

fig. 5a

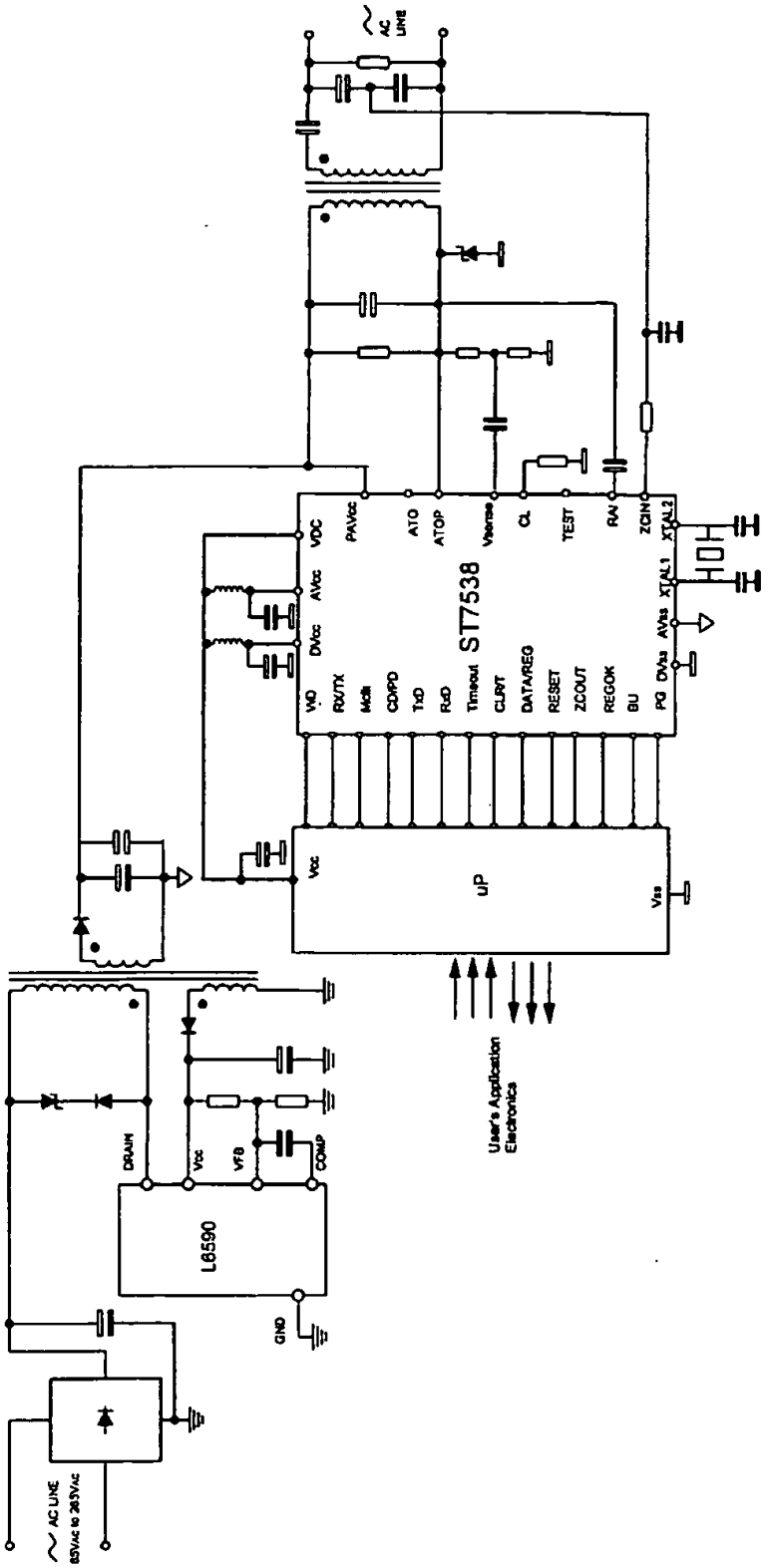
AC LINE
ST7538
VDC
PAVcc
ATO
ATOP
Vsense
CL
TEST
RAV
ZCIN
XTAL2
XTAL1
AVss
DVss
AVcc
DVcc
WD
RX/TX
Mdk
CDPD
TxD
RxD
Timeout
CLRT
DATAVREG
RESET
ZCOUT
REGOK
BU
PG
uP
Vcc
Vss
User's Application Electronics
L6590
DRAIN
Vcc
VFB
COMP
GND
AC LINE
85Vac to 265Vac

fig. 5b

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 83 0680

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	WO 94 03002 A (COMSOURCE SYSTEMS CORP ;HILL LAWRENCE WOODBRIDGE (US)) 3 February 1994 (1994-02-03)	1,2	H04B3/54
Y	* page 11, line 14 - page 12, line 13 * * page 19, line 15 - page 21, line 16; figure 11 * * page 27, line 2 - page 29, line 11 * * claim 7 *	3	
Y	EP 0 634 842 A (ABB PATENT GMBH) 18 January 1995 (1995-01-18) * abstract; claim 12 *	3	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H04B
G06F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	16 March 2000	De Iulis, N

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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16-03-2000

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		AU 4781393 A	14-02-1994
		EP 0651925 A	10-05-1995
EP 0634842 A	18-01-1995	DE 4323376 A	19-01-1995

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82